

FIG. 1

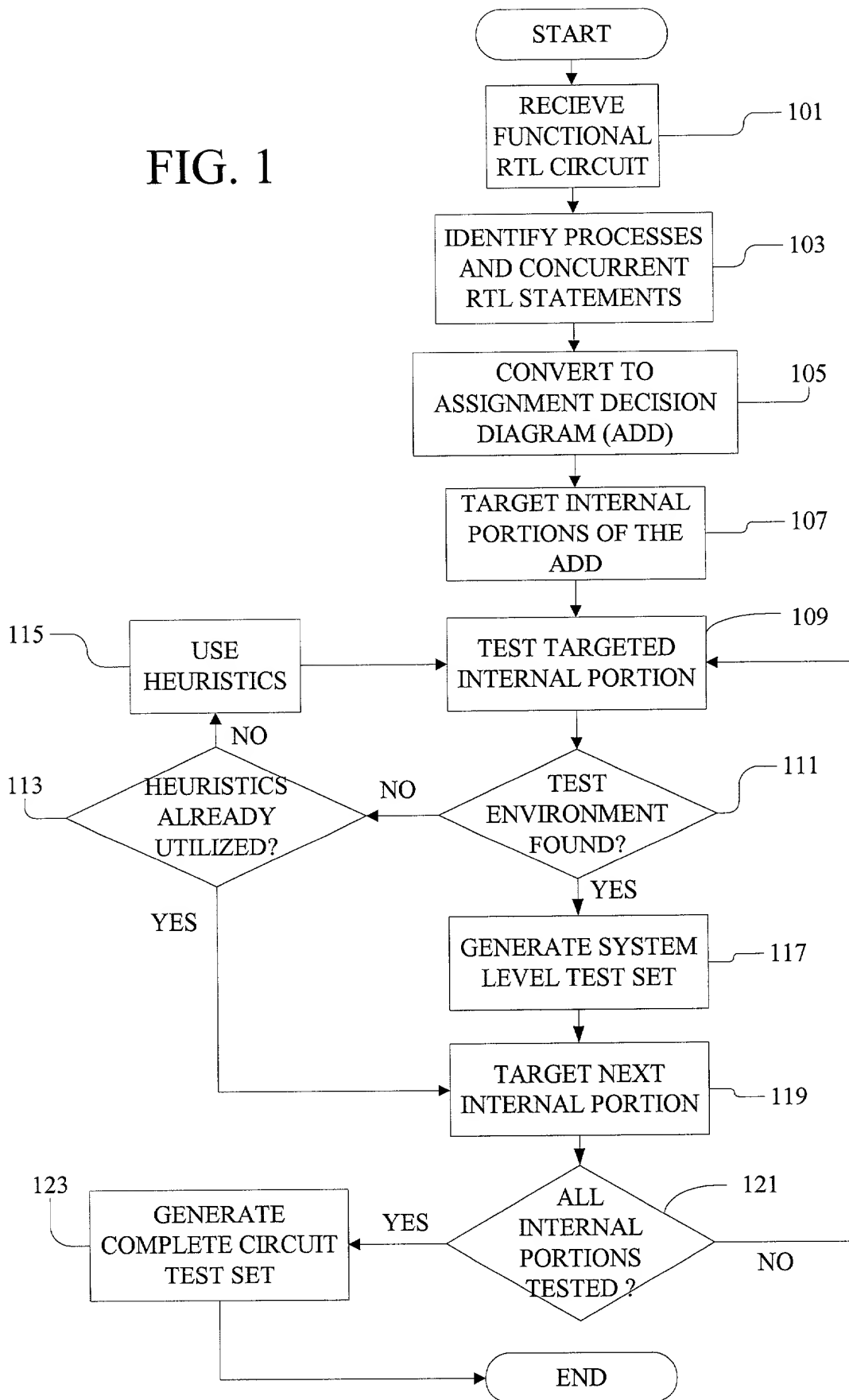


FIG. 2 is a block diagram of a logic circuit 20. The circuit 20 includes a first logic block 23, a second logic block 25, and a third logic block 27. The first logic block 23 includes registers R3, R4, R5, and R6. Register R3 contains the value 'a', register R4 contains the value '7', register R5 is a STATE REGISTER, and register R6 contains the value 'ST0'. The first logic block 23 also includes logic elements: a less-than operator (<) receiving inputs from R3 and R4, an equals operator (=) receiving inputs from R5 and R6, a NOT operator (!) receiving input from the less-than operator, an AND operator (&) receiving inputs from the less-than operator and the equals operator, and another AND operator (&) receiving inputs from the NOT operator and the first AND operator. The output of the first AND operator is labeled O3, the output of the NOT operator is labeled O5, the output of the first AND operator is labeled O6, and the output of the second AND operator is labeled O7. The second logic block 25 includes registers R1 and R2. Register R1 contains the value 'P' and register R2 contains the value 'Q'. The second logic block 25 also includes logic elements: a subtraction operator (-) receiving inputs from R1 and R2, and an addition operator (+) receiving inputs from R1 and R2. The output of the subtraction operator is labeled O1 and the output of the addition operator is labeled O2. The third logic block 27 includes a multiplexer ADN1 and a register R. The multiplexer ADN1 has two inputs labeled AI1 and AI2, and its output is labeled W11. The register R is connected to the output of the multiplexer ADN1. The first logic block 23 is connected to the second logic block 25 via signals AS1 and AS2. The second logic block 25 is connected to the third logic block 27 via signal 21. The third logic block 27 is connected to the first logic block 23 via signal 25.

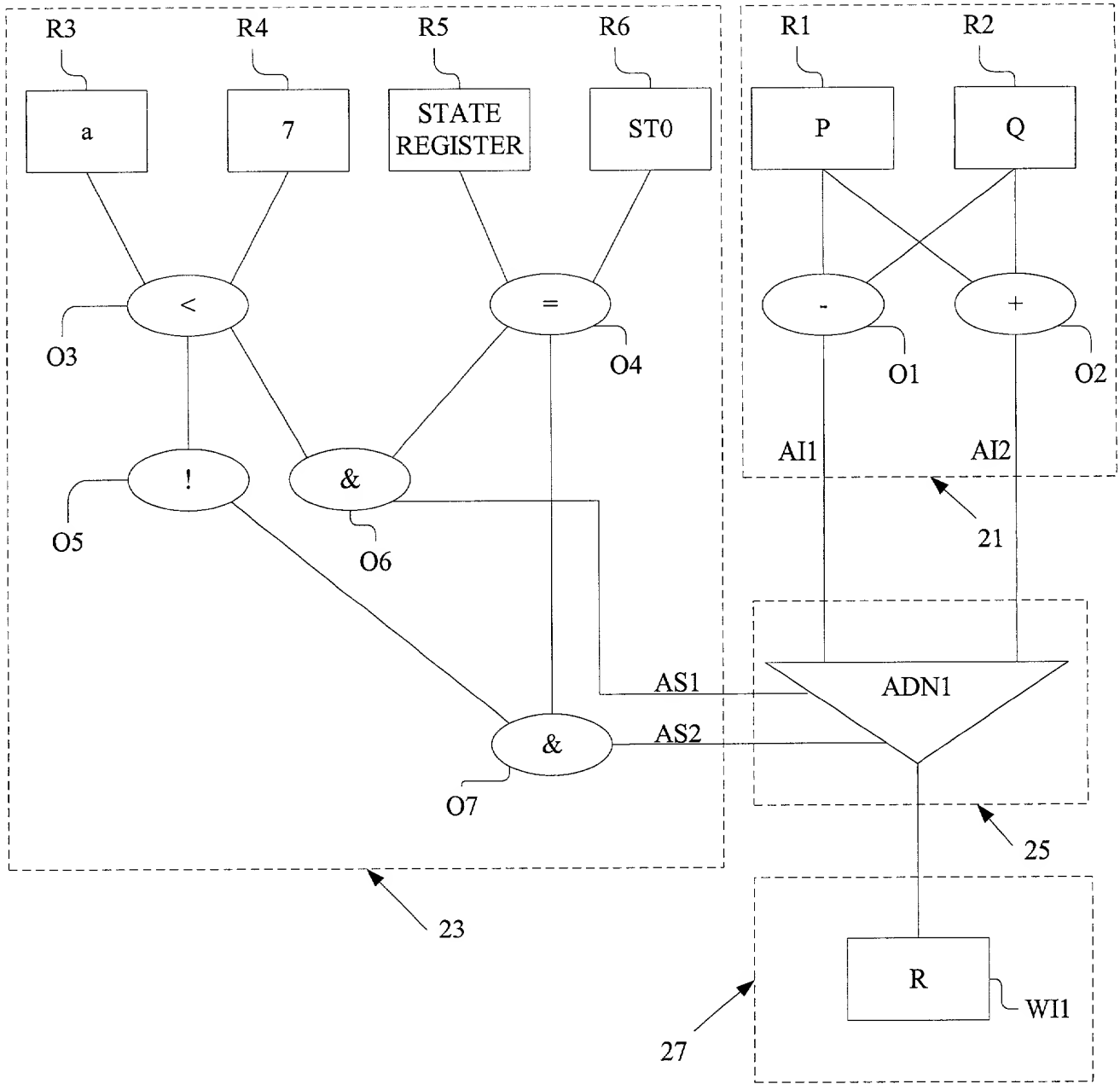


FIG. 2

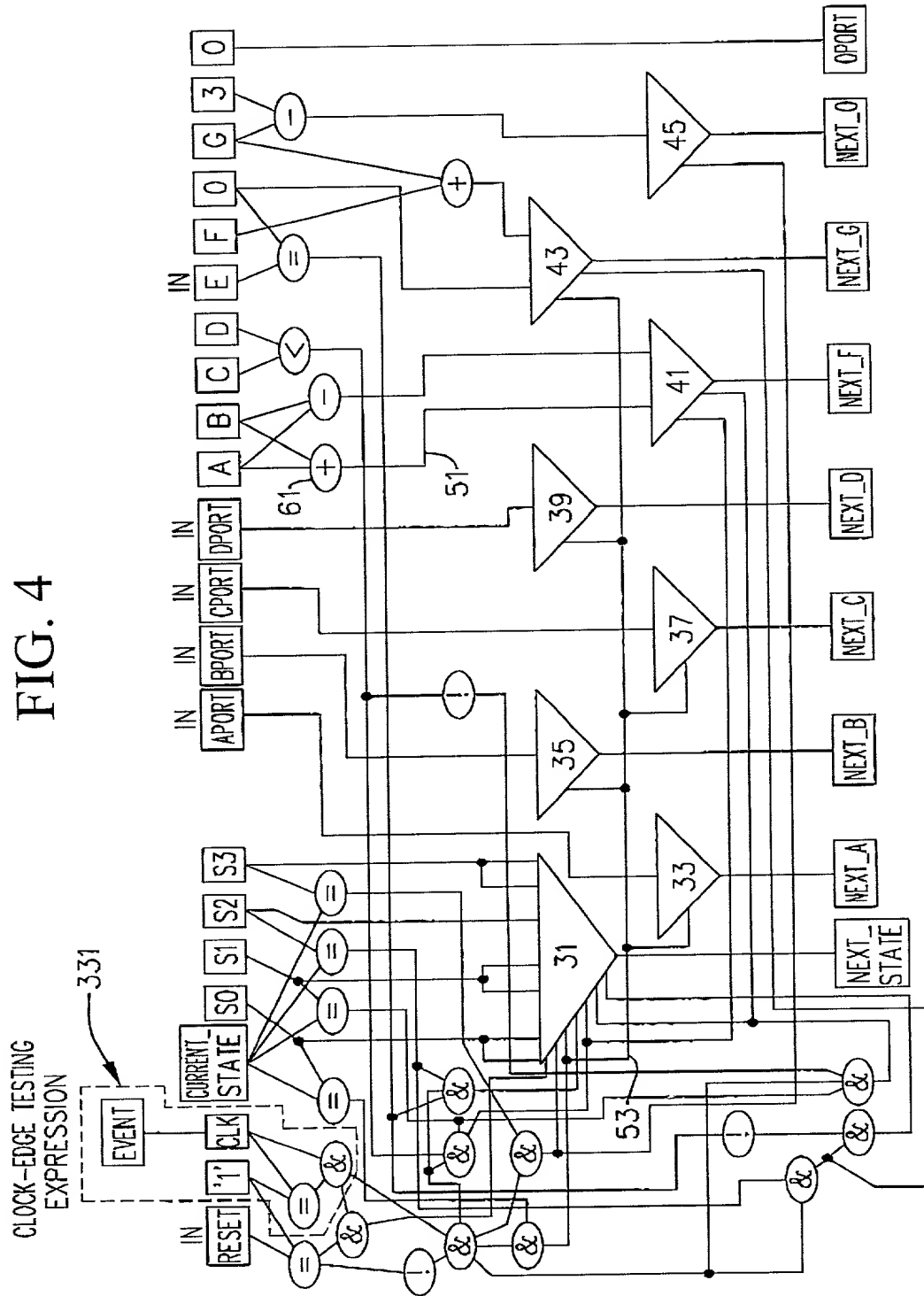
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entity T1 is
  port ( RESET, CLK :IN std_logic;
        APORT, BPORT, CPORT, DPORT : IN std_logic_vector (7 downto 0);
        E : IN std_logic;
        OPORT : OUT std_logic_vector (7 downto 0) );
  end T1;
architecture RTL of T1 is
  type STATE_TYPE is ( S0, S1, S2, S3);
  signal CURRENT_STATE, NEXT_STATE : STATE_TYPE;
  SIGNAL A, B, C, D, F, G, O, NEXT_A, NEXT_B, NEXT_C, NEXT_D,
        NEXT_F, NEXT_G, NEXT_O : std_logic_vector (7 downto 0);
  begin
    COMBIN : process (CURRENT_STATE)
      begin
        NEXT_A <= A; NEXT_B <= B; NEXT_C <= C; NEXT_D <= D;
        NEXT_F <= F; NEXT_G <= G; NEXT_O <= O; OPORT <= O;
        case CURRENT_STATE is
          when S0 =>
            NEXT_A <= APORT; NEXT_B <= BPORT;
            NEXT_C <= CPORT; NEXT_D <= D;
            NEXT_G <= "00000000";
          when S1 =>
            if ( C < D ) then
              NEXT_F <= A + B;
              NEXT_STATE <= S2;
            else
              NEXT_F <= A - B;
              NEXT_STATE <= S3;
            end if;
          when S2 =>
            NEXT_G <= F + G;
            if ( E = '0' ) then
              NEXT_STATE <= S1;
            else
              NEXT_STATE <= S3;
            end if;
          when S3 =>
            NEXT_O <= G - 3;
            NEXT_STATE <= S0;
          end case;
        end process;
    SYNCH : process (CLK, RESET)
      begin
        if ( CLK'event and CLK = '1' ) then
          if ( RESET = '1' ) then
            CURRENT_STATE <= S0;
          else
            A <= NEXT_A; B <= NEXT_B; C <= NEXT_C; D <= NEXT_D;
            G <= NEXT_G; F <= NEXT_F; O <= NEXT_O;
          end if;
        end if;
      end process;
  end RTL;

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FIG. 3

FIG. 4



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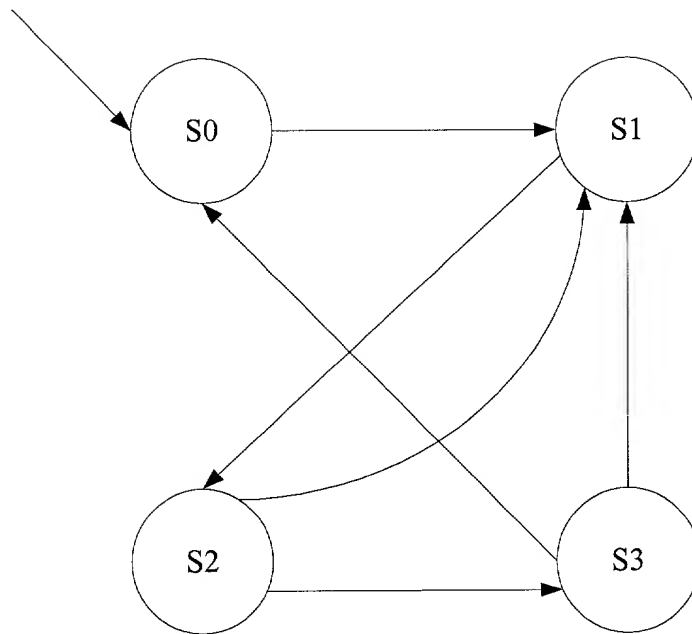


FIG. 5

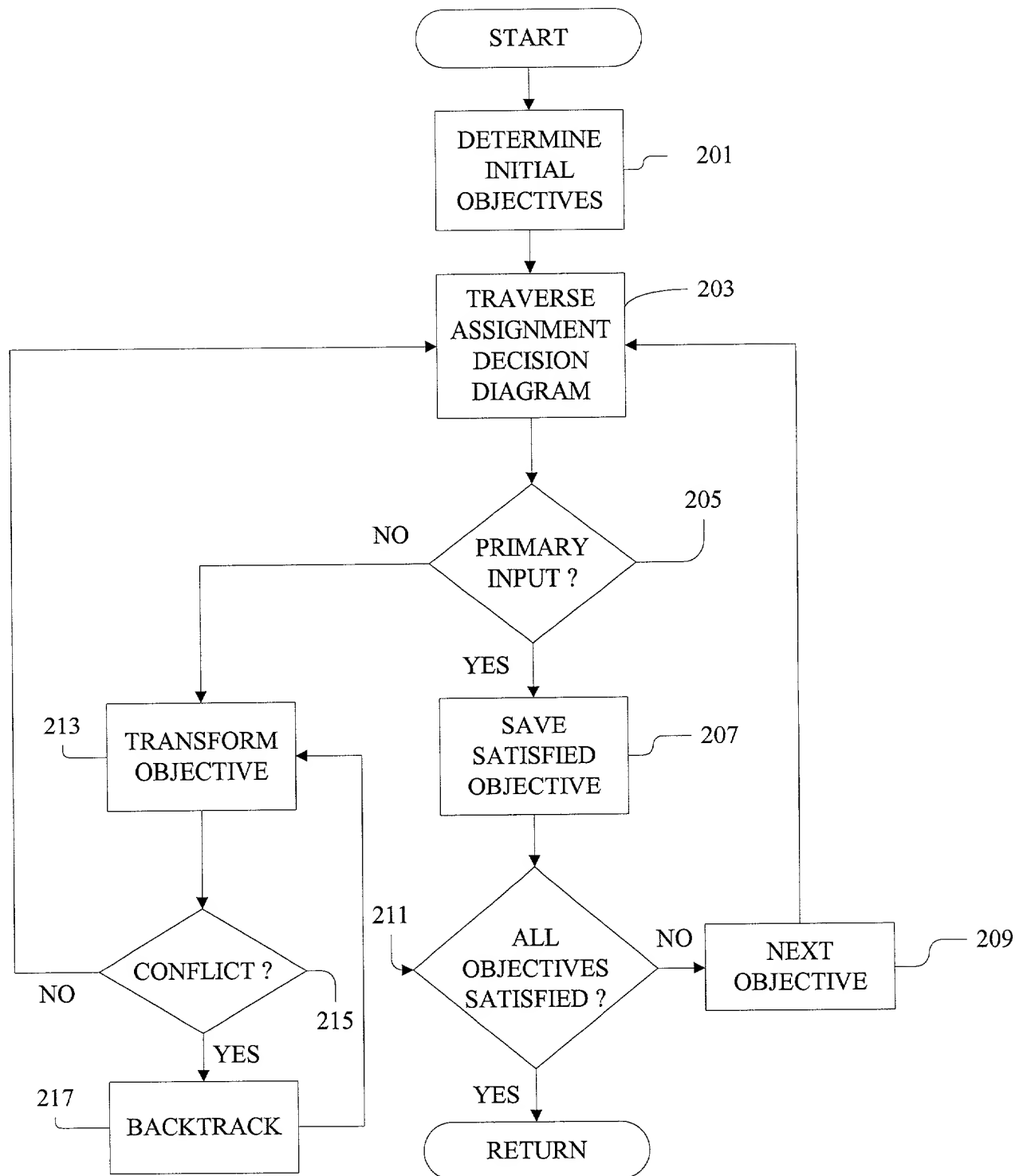


FIG. 6

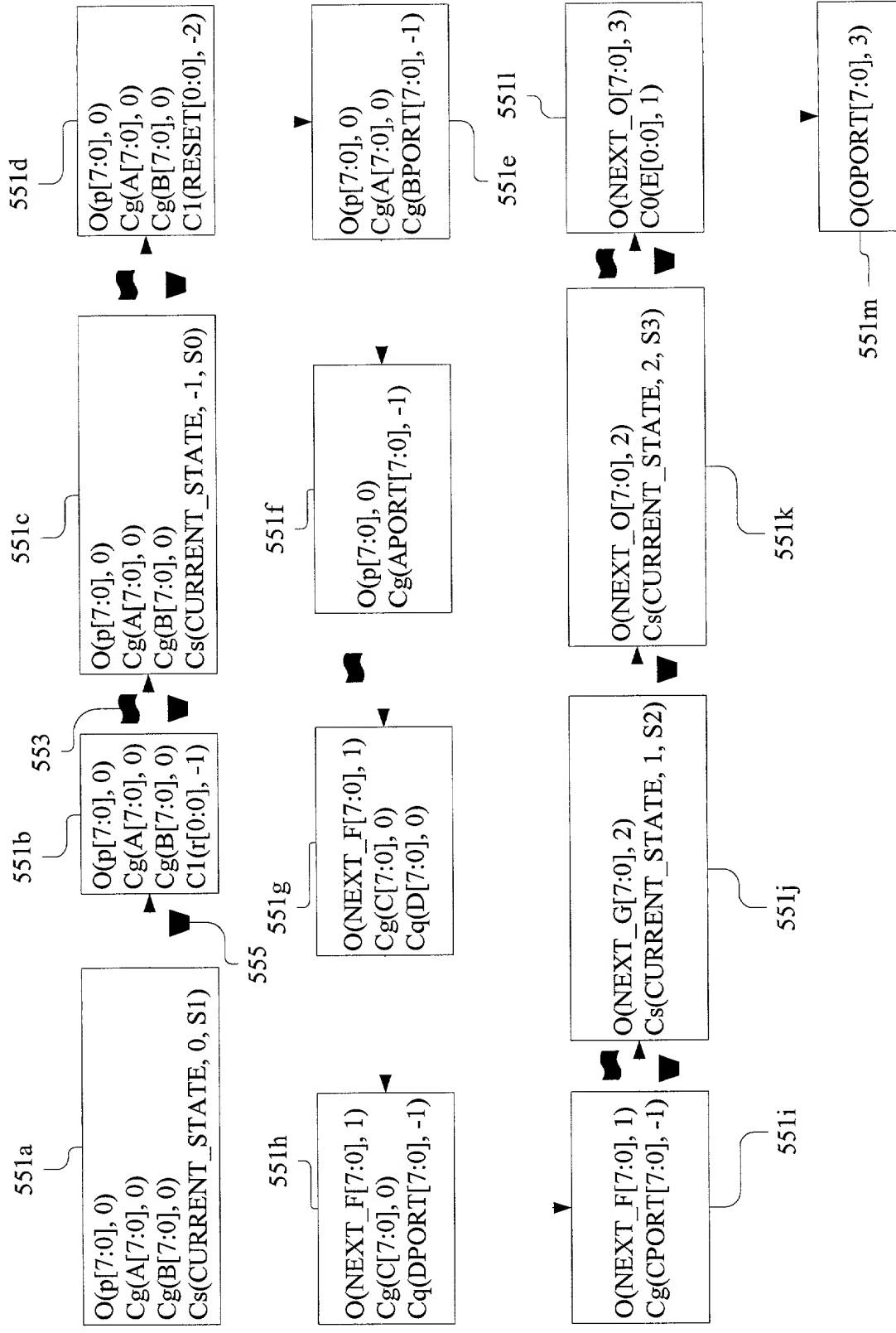


FIG. 7

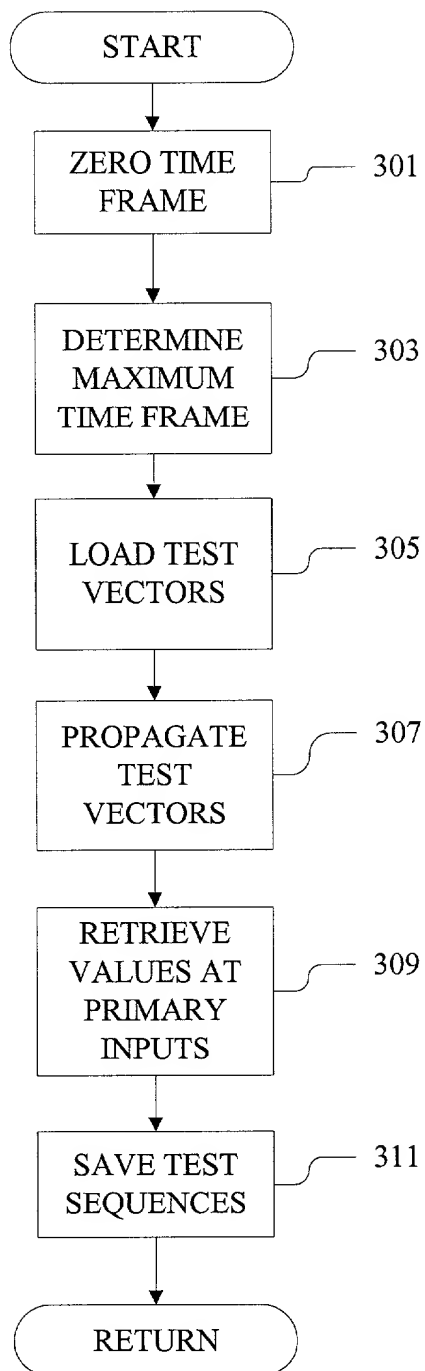


FIG. 8



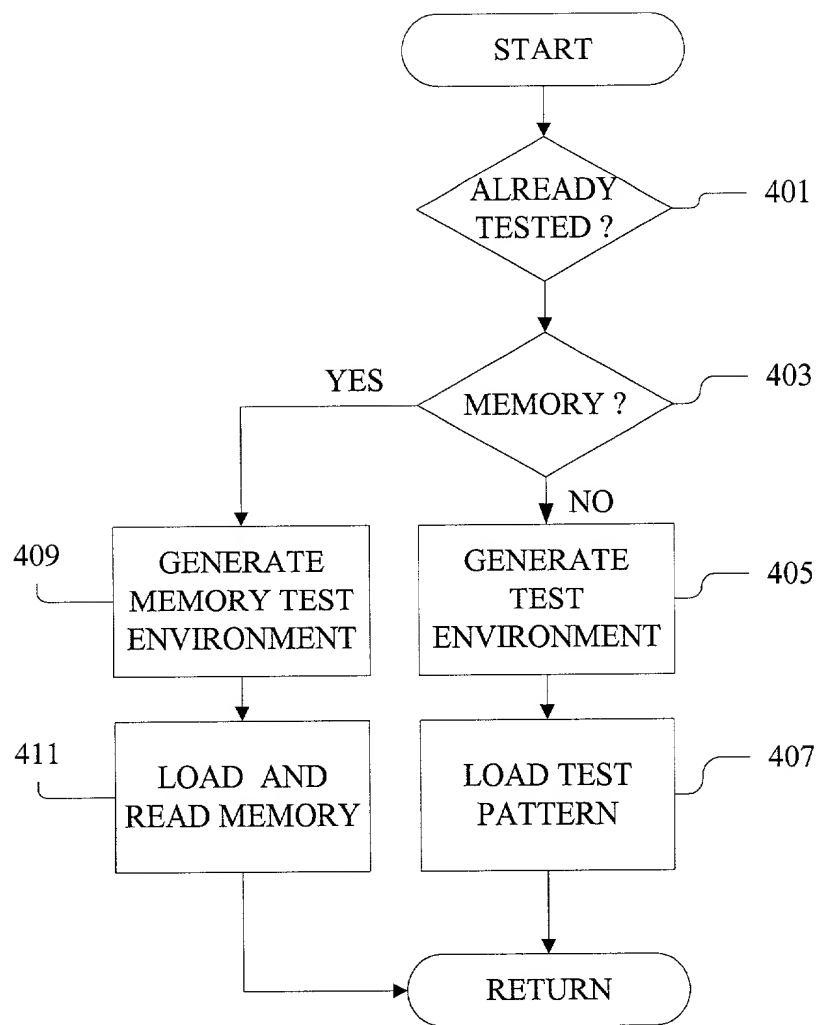


FIG. 9

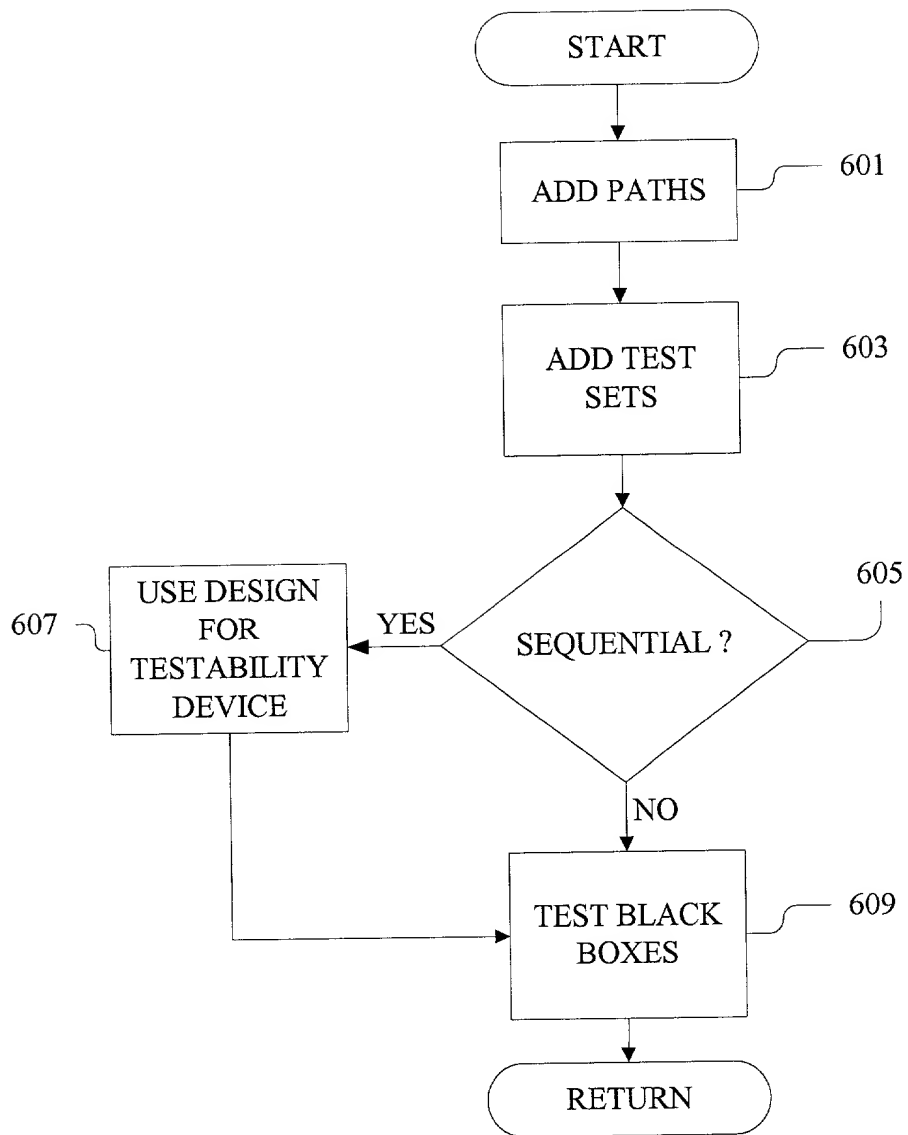


FIG. 10